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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,226	12/10/2003	William M. Hiatt	108298744US	8010

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PERKINS COIE LLP
PATENT-SEA
P.O. BOX 1247
SEATTLE, WA 98111-1247

EXAMINER	
MATTHEWS, COLLEEN ANN	
ART UNIT	PAPER NUMBER
2811	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/733,226	HIATT ET AL.	
	Examiner	Art Unit	
	Colleen A. Matthews	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 28-52* is/are pending in the application.

4a) Of the above claim(s) *12-14 and 37* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11, 28-36 and 38-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/14/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Applicant's election without traverse of species Embodiment 2, shown in Figures 5A-5B in reply filed on 06/21/2006 corresponds to claims 1-11, 28-36 and 38-47 and new claims 48-52 filed 11/10/2006.

Specification

The attempt to incorporate subject matter into this application by reference to a related U.S. Patent Application is ineffective because the application number is not provided in paragraph [0001].

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 1, 6-10, 28-30, 33, 36, 38-42, 44-45 and 48-52** are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Pat. No. 6,703,310 to Mashino et al. (Mashino).

3. **Regarding claim 1,** Mashino discloses a method of forming a conductive interconnect in a microelectronic device, the method comprising: providing a

microfeature workpiece (Figures 1-8, element 215) having a plurality of dies; forming a passage (212) extending through the microfeature workpiece from a first side (201a) of the microfeature workpiece to an opposite second side (201b) of the microfeature workpiece; forming a conductive plug (Fig 7/8 element 214)in the passage adjacent to the first side of the microelectronic workpiece; and depositing conductive material (Fig 7/8 element 217) in the passage to at least generally fill the passage from the conductive plug to the second side of the microelectronic workpiece.

4. **Regarding claim 6,** Mashino discloses the method of claim 1, further comprising forming a bond-pad (211) on the microelectronic workpiece, wherein forming the passage (212) includes forming the passage through the bond-pad (Figure 4L), and wherein forming a conductive plug in the passage includes depositing a conductive material to contact an exposed surface of the bond-pad (col 6 lines 65-67).

5. **Regarding claim 7,** as far as the claim can be understood, Mashino discloses the method of claim 1 where forming the passage includes laser drilling (Figure 4L, col 9 line 37- col 10 line 4) the passage through the die.

6. **Regarding claim 8**, Mashino discloses the method of claim 1 where providing a microfeature workpiece includes providing a die having an integrated circuit (202) and a bond-pad (211) electrically coupled to the integrated circuit (col 6 lines 50-52), and wherein forming the passage (212) includes laser drilling (Figure 4L, col 9 line 37- col 10 line 4) the passage through the die and the bond pad (col 6 lines 58-59).

7. **Regarding claim 9**, Mashino discloses the method of claim 1, further comprising applying a passivation layer (204) to at least a portion of the passage before forming the

conductive plug in the passage and filling the passage from the conductive plug (214) to the second side (201b) of the microelectronic workpiece.

8. **Regarding claim 10,** Mashino discloses the method of claim 1 further comprising forming a bond-pad (211) on the microelectronic workpiece in contact with the conductive plug (col 6 lines 65-67).

9. **Regarding claim 11,** Mashino discloses the method of claim 1 where depositing conductive material in the passage to at least generally fill the passage includes biasing the conductive plug at an electrical potential (power feed layer 205a, can provide an electrical potential).

10. **Regarding claim 28,** Mashino discloses a packaged microelectronic device (Figures 1-8, element 215) comprising: a die having a first side (201a) and a second side (201b) opposite to the first side, the die further having an integrated circuit (202) positioned between the first and second sides; a bond-pad (211) positioned on the first side of the die and electrically coupled to the integrated circuit (col 6 lines 50-52); a passage (212) extending completely through the die and aligned with the bond-pad; a first conductive material (214) deposited in a first portion of the passage adjacent to the first side of the die to form a conductive plug electrically connected to the bond-pad (col 6 lines 65-67); and a second conductive material (217) deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage from the conductive plug to the second side of the die.

11. **Regarding claim 29,** Mashino discloses the packaged microelectronic device of claim 28, further comprising an insulative layer (209) deposited in the passage (212) between the die and the first and second conductive materials.

12. **Regarding claim 30,** Mashino discloses the packaged microelectronic device of claim 28 wherein the passage (212) extends through the bond-pad (col 6 lines 58-59), and further comprising an insulative layer (209) deposited in the passage between the die and the first and second conductive materials.

13. **Regarding claim 33**, Mashino discloses a microfeature workpiece having a first side (201a) and a second side (210b) opposite to the first side, the microfeature workpiece comprising: at least one die; a passage (212) extending completely through the die from the first side of the microfeature workpiece to the second side of the microfeature workpiece; a first conductive material (214) deposited in a first portion of the passage adjacent to the first side of the microfeature workpiece to form a conductive plug; and a second conductive material (217) deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage from the conductive plug to the second side of the microfeature workpiece.

14. **Regarding claim 36,** Mashino discloses the microfeature workpiece of claim 33, further comprising an insulative layer (209) deposited in the passage (212) between the die and the first and second conductive materials.

15. **Regarding claim 38**, Mashino discloses the microfeature workpiece of claim 33, further comprising a bond- pad (211) formed on the first side of the microfeature workpiece in contact with the conductive plug (col 6 lines 65-67).

16. **Regarding claim 39**, Mashino discloses a microelectronic device set (Figure 8) comprising: a first microelectronic device (215) having a first die with a first integrated circuit (202) and a first bond-pad (211) electrically coupled to the first integrated circuit (col 6 lines 50-52), the first die further including a passage (212) extending completely through the first die and the first bond-pad (col 6 lines 58-59); and a conductive interconnect deposited in the passage, the conductive interconnect including a first conductive material (214) deposited in a first portion of the passage to form a conductive plug, and a second conductive material (217) deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage; and at least a second microelectronic device (Fig 8, another element 215) having a second die with a second integrated circuit (202) and a second bond-pad (211) electrically coupled to the second integrated circuit (col 6 lines 50-52), wherein the second bond-pad is electrically coupled to the conductive interconnect of the first microelectronic device (col 7 line 62-col 8 line 15).

17. **Regarding claim 40**, Mashino discloses the microelectronic device set of claim 39 wherein the first microelectronic device is attached to the second microelectronic device in a stacked-die arrangement (Fig 8, col 7 line 62-col 8 line 15).

18. **Regarding claim 41**, Mashino discloses the microelectronic device set of claim 39, further comprising a solder ball (210) disposed between the conductive interconnect of the first microelectronic device and the second bond-pad of the second microelectronic device to electrically couple the first bond-pad to the second bond-pad (Fig 8, col 7 line 62-col 8 line 15).

19. **Regarding claim 42**, Mashino discloses the microelectronic device set of claim 39 wherein the passage is a first passage (212), wherein the second microelectronic device further includes a second passage (212) extending through the second die and the second bond-pad (211), and wherein the second passage is completely filled with a third conductive material (217).

20. **Regarding claim 44**, Mashino discloses a microelectronic device set (Figure 8) comprising: a first microelectronic device (215) having a first die with a first integrated circuit (202) and a first bond-pad (211) electrically coupled to the first integrated circuit (col 6 lines 50-52), the first die further including a passage (212) aligned with the first bond-pad; and a conductive interconnect deposited in the passage, the conductive interconnect including a first conductive material (214) deposited in a first portion of the passage to form a conductive plug in contact with the bond-pad (col 6 lines 65-67), and a second conductive material (217) deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage; and at least a second microelectronic device (Fig 8 another element 215) having a second die with a second integrated circuit (202) and a second bond-pad (211) electrically coupled to the second integrated circuit(col 6 lines 50-52), wherein the second bond-pad is electrically coupled to the first bond-pad of the first microelectronic device (col 7 line 62 – col 8 line 15).

21. **Regarding claim 45**, Mashino discloses the packaged microelectronic device of claim 44, further comprising an insulative layer (209) deposited in the passage (212) between the die and the first and second conductive materials.

22. **Regarding claim 48**, Mashino discloses the method as above, comprising applying a passivation layer (209) to at least a portion of the passage before forming the conductive plug (214) in the passage, and depositing conductive material (217) in the passage (212) to at least generally fill the passage includes depositing the conductive material in contact with the conductive plug (214) and the passivation layer (209).

23. **Regarding claims 49-52,** Mashino discloses the device as above, further comprising an insulative layer (209) deposited in the passage (212), where the second conductive material (217) contacts the conductive plug (214) and insulative layer (209).

Claim Rejections - 35 USC § 103

24. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

25. **Claim 2** is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,703,310 to Mashino et al. (Mashino) in view of U.S. Pat. No. 7,045,015 to Renn et al. (Renn).

26. **Regarding claim 2,** Mashino discloses the method of claim 1, as above, and forming a conductive plug by depositing an electrically conductive material in the passage. Mashino lacks disclosing depositing an electrically conductive material by using a maskless mesoscale materials deposition process. Renn discloses using a maskless mesoscale materials deposition process to deposit an electrically conductive

material (col 8 lines 24-26). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Mashino to have the electrically conductive material deposited by a maskless mesoscale materials deposition process as in Renn because the process can deposit fine features on low-temperature or high-temperature substrates (col 2 lines 22-25).

27. **Claims 3, 31, and 34** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,703,310 to Mashino et al. (Mashino) in view of U.S. Pub. No. 2004/0087441 to Hirakata et al. (Hirakata).

28. **Regarding claims 3, 31, 34 and 46,** Mashino discloses the method of claims 1, 28, 33 and 44 as above. Mashino discloses the passage extends through the bond-pad and the first conductive material in contact with an exposed surface of the bond pad. Mashino lacks disclosing forming a conductive plug includes applying an electronic ink in the passage using an electronic printing process. Hirakata teaches forming a conductive plug includes applying an electronic ink (conductive paste; paragraph 102) in the passage using an electronic printing process (ink jetting; paragraph 102). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the conductive e plug by applying an electronic ink using an electronic printing process as in Hirkata because with electronic printing processes the plug only needs to be formed in the desired area therefore wasted material is reduced.

29. **Claims 4, 32, 35 and 47** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,703,310 to Mashino et al. (Mashino) in view of U.S. Pub. No. 2004/0087441 to Bock et al. (Bock).

30. **Regarding claims 4, 32, 35, and 47,** Mashino discloses the method of claims 1, 28, 33 and 44 as above. Mashino also discloses forming a conductive plug includes depositing an electrically conductive material in the passage, and the passage extends through the bond-pad and the first conductive material is in contact with an exposed surface of the bond pad.

Mashino lacks disclosing depositing an electrically conductive material using a nano-particle deposition process. Bock teaches using a nano-particle process to deposit a conductive material (abstract lines 15-20). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Mashino to have the electrically conductive material deposited by a nano-particle process as in Bock because the process can deposit fine features.

31. **Claim 5** is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,703,310 to Mashino et al. (Mashino) in view of U.S. Pat. No. 6,828,223 to Chuang.

32. **Regarding claim 5,** Mashino discloses the method of claim 1 where forming a conductive plug includes depositing a metal into the passage (copper, col 7 lines 28-29). Mashino lacks discloses the metal as silver. Chuang teaches using silver as a conductive plug (col 1 lines 11-21). It would have been obvious to one of ordinary skill in

the art at the time the invention was made to modify Mashino to have the metal be silver as in Chuang because silver has low-resistivity and is a good electrical conductor.

33. **Claim 43** is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,703,310 to Mashino et al. (Mashino) in view of applicant's Admitted Prior Art (APA).

34. **Regarding claim 43**, Mashino disclose the microelectronic device set of claim 39 as above. Mashino lacks discloses the first microelectronic device further includes a redistribution layer formed on the first die, the redistribution layer including a conductive line having a first end portion attached to the first bond-pad and a second end portion positioned outward of the first end portion, wherein the second end portion is configured to receive electrical signals and transmit the signals to at least the first integrated circuit of the first die and the second integrated circuit of the second die.

APA teaches the first microelectronic device further includes a redistribution layer (Figure 1 element 28) formed on the first die, the redistribution layer including a conductive line having a first end portion (side near solder ball 21) attached to the first bond-pad and a second end portion (other side near solder ball 21) positioned outward of the first end portion, wherein the second end portion is configured to receive electrical signals and transmit the signals to at least the first integrated circuit of the first die and the second integrated circuit of the second die.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Mashino to include a redistribution layer as in the APA in order to provide connections between the dies.

Response to Arguments

Applicant's arguments, see page 10 section A, filed 11/10/2006, with respect to claim 7 have been fully considered and are persuasive. The 35 USC 112 rejection of claim 7 has been withdrawn.

Applicant's remaining arguments filed 11/10/2006 have been fully considered but they are not persuasive.

Applicant argues that Mashino's interconnection pattern 214 does not plug the through hole *after* the interconnection pattern is applied because the statement that "the through hole 212 is hollow" in Mashino col 7 lines 25-26 (Remarks, page 12, lines 3-5). The examiner respectfully disagrees, because as shown in Figure 4L, through hole 212 is first defined as the hollow, open area, between segments of silicon substrate 201, when layer 214 is not present.

Applicant argues that Mashino's interconnection pattern 214 does not plug the through hole 212 (Remarks, page 12, lines 3-15). However, the examiner maintains the position that Mashino's layer 214 can be considered a "conductive plug".

The term "conductive plug" is interpreted broadly in accordance with MPEP 2106, *USPTO personnel are to give claims their broadest reasonable interpretation in light of*

the supporting disclosure. In re Morris, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997).

Applicant recites the dictionary definition of "a plug" including the definition of "a dense mass of material that obstructs a passage" (Remarks, page 12, lines 10-11). Mashino's layer 214, is a dense mass of material. The definition of plug provided by the applicant does not in any way limit the degree to which the passage must be obstructed. The passage, as considered as the open area between segments of silicon substrate 201, is narrower as a result of the presence of the material of 214, therefore material 214 obstructs the passage. Because the material 214 is "a dense mass of material that obstructs a passage" it can be considered a plug.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colleen A. Matthews whose telephone number is 571-272-1667. The examiner can normally be reached on Monday - Friday 8AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CAM
01/23/2007

Sara Crane
Primary Examiner